Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-44 (cancelled)

Claim 45 (previously presented): A method involving a first line card, a second line card, and a switch fabric, the first line card comprising an ingress device and an egress device, the second line card comprising an ingress device and an egress device, a flow of network information flowing out of the ingress device of the first line card and through the switch fabric and to the egress device of the second line card, the egress device of the second line card having an amount of payload memory available for storing network information, wherein the egress device of the second line card comprises a first integrated circuit, the ingress device of the second line card comprises a second integrated circuit, the egress device of the first line card comprises a third integrated circuit, and the ingress device of the first line card comprises a fourth integrated circuit, wherein the first, second, third and fourth integrated circuits are substantially structurally identical integrated circuits, the method comprising:

(a) detecting on the egress device of the second line card that the amount of available payload memory has reached a low level;

(b) in response to the detecting of (a) sending a first indication from the egress device of the second line card to the ingress device of the second line card, the first indication being sent from the egress device of the second line card to the ingress device of the second line card via a bus on the second line card;

(c) receiving the first indication on the ingress device of the second line card and in response sending a status switch cell from the ingress device of the second line card, through the switch fabric, and to the egress device of the first line card;

(d) receiving the status switch cell on the egress device of the first line card and in

response sending a second indication from the egress device of the first line card to the ingress device of the first line card, the second indication being sent for the egress device of the first line card to the ingress device of the first line card via a bus on the first line card; and

(e) receiving the second indication on the ingress device of the first line card and in response slowing the flow of the network information out of the ingress device of the first line card.

Claim 46 (previously presented): The method of Claim 45, wherein the payload memory is coupled to the egress device of the second line card.

Claim 47 (previously presented): The method of Claim 45, wherein the bus on the second line card is a serial bus, and wherein the bus on the first line card is a serial bus.

Claim 48 (previously presented): The method of Claim 45, wherein the flow of the network information is slowed in (e) by stopping the flow of the network information out of the ingress device of the first line card.

Claim 49 (previously presented): The method of Claim 45, wherein the egress device of the second line card maintains a free buffer queue, the free buffer queue having a size, the egress device of the second line card detecting that the amount of available payload memory has reached a low level in (a) by monitoring the size of the free buffer queue.

Claim 50 (cancelled)

Claim 51 (previously presented): The method of Claim 45, wherein each of the first, second, third and fourth integrated circuits is an integrated circuit that has a single data path, the single data path extending from a first bus interface, through segmentation circuitry, through reassembly circuitry, and to a second bus interface.

Claim 52 (previously presented): The method of Claim 45, wherein the ingress device of the

first line card is a multi-service segmentation and reassembly device, the multi-service segmentation and reassembly device receiving both flows of packets and flows of cells.

Claim 53 (currently amended): A system, comprising:

a switch fabric;

a first line card comprising an ingress device and ~~en~~ an egress device, the ingress device of the first line card being coupled to the egress of the first line card via a first serial bus; and

a second line card comprising an ingress device and an egress device, the ingress device of the second line card being coupled to the egress device of the second line card via a second serial bus, the egress device of the second line card backpressuring the ingress device of the first line card by sending a backpressuring signal to the ingress device of the first line card, the backpressuring signal passing from the egress device of the second line card to the ingress device of the second line card via the second serial bus, the backpressuring signal then passing from the ingress device of the second line card to the egress device of the first line card in the form of a status switch cell passed from the ingress device of the second line card to the egress device of the first line card through the switch fabric, the backpressuring signal then passing from the egress device of the first line card to the ingress device of the first line card via the first serial bus,

wherein the egress device of the second line card comprises a first integrated circuit, the ingress device of the second line card comprises a second integrated circuit, the egress device of the first line card comprises a third integrated circuit, and the ingress device of the first line card comprises a fourth integrated circuit, wherein the first, second, third and fourth integrated circuits are substantially structurally identical integrated circuits.

Claim 54 (previously presented): The system of Claim 53, wherein a flow of network information passes from the ingress device of the first line card, through the switch fabric, and to the egress device of the second line card, and wherein the ingress device of the first line card receives the backpressuring signal and in response thereto shows the flow of network information.

Claim 55 (previously presented): The system of Claim 53, wherein the egress device of the second line card maintains a free buffer queue, the free buffer queue having a size, the egress device of the second line card sending the backpressuring signal via the second serial bus if the egress device of the second line card determines that the size of the free buffer queue has reached a low level.

Claim 56 (cancelled)

Claim 57 (previously presented): The system of Claim 53, wherein each of the first, second, third and fourth integrated circuits is an integrated circuit that has a single data path, the single data path extending from a first bus interface, through segmentation circuitry, through reassembly circuitry, and to a second bus interface.

Claims 58-59 (cancelled)